NVL IR-ATR : Round 0

UCLA / USC ISI

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1. Overview

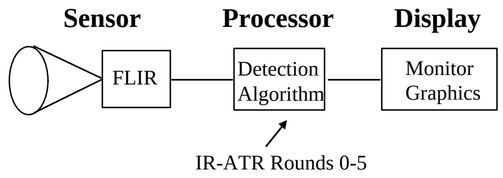
Design Challenge

- Night Vision Laboratories has developed a template matching algorithm for infrared spectral images.
- Application is real-time target cueing system for M1 tank in nighttime operations.
- The NVL algorithm is a 6-level decision tree, with the top level (Round 0) comprising the largest computation bottleneck.

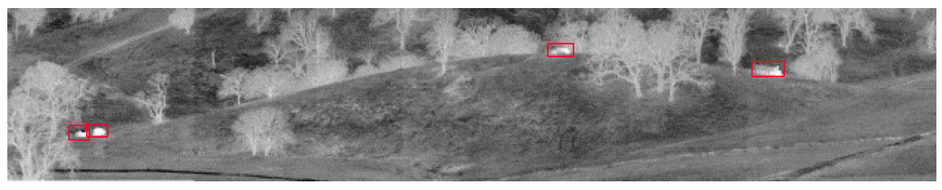
Team Effort

- UCLA and USC/ISI have partnered to build an FPGA-based implementation for the Round 0 algorithm.
- UCLA has developed a Round 0 implementation in VHDL which will be used to configure the FPGAs on the SLAAC II board, developed by USC/ISI.

2. Image Cueing System



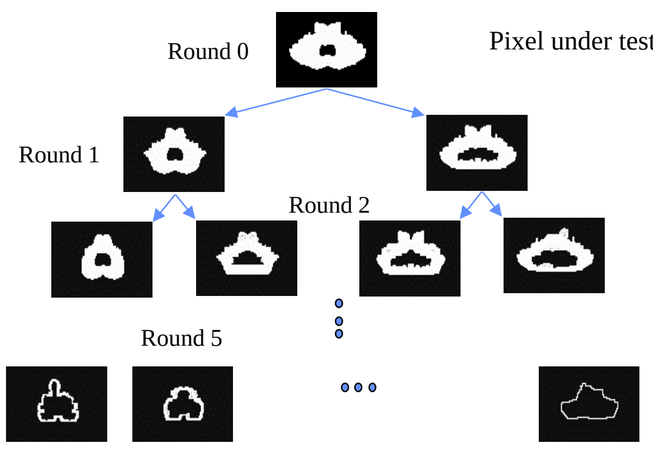
- Tank operator sees infrared image displayed on monitor, with areas of high target probability marked with boxes.



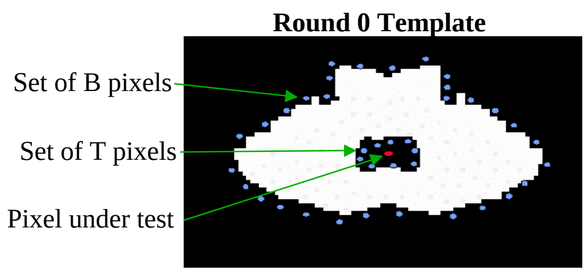
- Time critical application: detection algorithms must be performed in less than 100ms for a refresh rate of 10 frames/sec.
- On board tank system has room for two 6U VME boards.

3. IR-ATR Templates

Operation: For each pixel under test, process background and target pixels according to R0 template, then pass the locations of those pixels that exceed R0 threshold for R1 processing, etc.

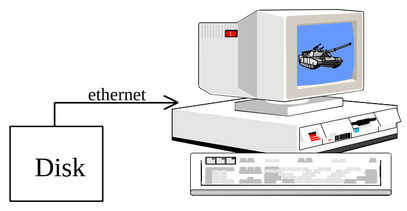


Round 0 Template



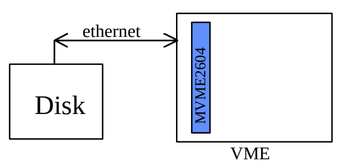
30 Background points (B pixels) and 30 Target points (T pixels) are chosen based on template

4. Timing Benchmarks



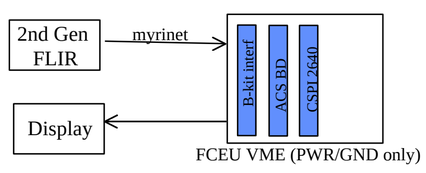
Sun workstation UltraSPARC 60, network data
Total time: 13.412461 s

R0:	12.844284s	R3:	0.074972s
R1:	0.291631s	R4:	0.022147s
R2:	0.179267s	R5:	0.000160s



Single MVME2604, PPC 604e, network data
Total time: 19.266664 s

R0:	18.366664s	R3:	0.183333s
R1:	0.299999s	R4:	0.050000s
R2:	0.366667s	R5:	0.000001s



Multiple CSPI 2640 PPC 603e, ACS R0, sensor data
Total time: < 0.1 s (May 99)

R0:	TBD	R3:	TBD
R1:	TBD	R4:	TBD
R2:	TBD	R5:	TBD

5. Round 0 Calculations

T is the value of a Target Pixel
B is a Background Pixel

M = Mean of Background Pixels

H = Σ(T-M) (for all T > M)

C = Σ(T-M) (for all T ≤ M)

D_H = Σ(B-M) (for all B > M)

D_C = Σ(M-B) (for all B ≤ M)

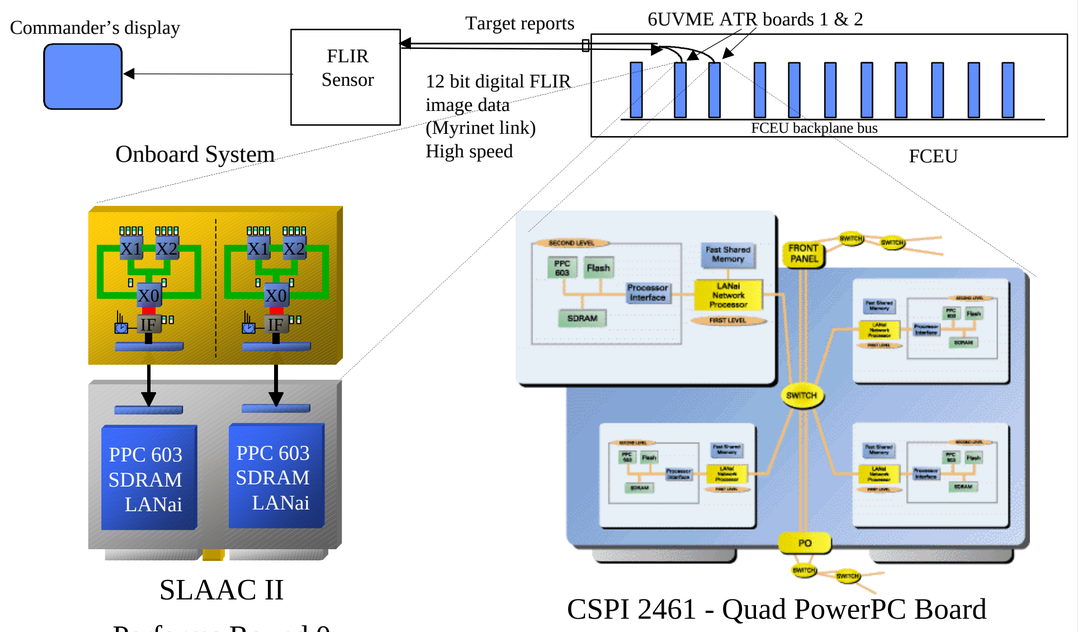
$S_H = (H-Dh)/(H+Dh)$

$S_C = (C-Dc)/(C+Dc)$

$R = \max(0, S_H^+ + S_C^+,)$

To exploit parallelism in the Round 0 algorithm, computations are split into macroblocks. The completion of the calculations in one macroblock takes 20 clock cycles (including latency inside macroblock). The 4 macroblocks are placed in a pipeline which loads each “macro cycle” (or every 20 clock cycles).

6. IR-ATR Hardware Overview



SLAAC II

Performs Round 0

CSPI 2461 - Quad PowerPC Board

Performs Rounds 1-5

7. SLAAC2 Architecture

SLAAC2

- Equivalent to two SLAAC1 boards.

Programmable Logic

- Xilinx XC40150XVfor X1, X2
- Xilinx XC4085XLA for X0
- Xilinx XC4085XL for IF
- >750K gates equivalent user logic.

I/O

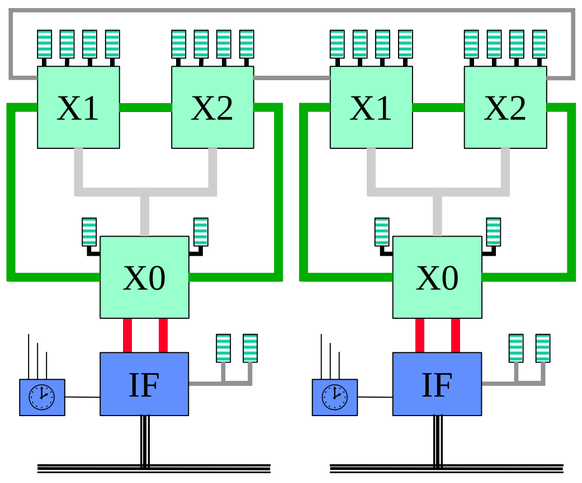
- 64-bit PowerPC bus at 40MHz.
- 64-bit data-paths throughout design.

Memory

- Ten 256Kx18 fast cache memories.

Speed

- User programmable clock to 100MHz.



8. Current Status

Upcoming Events

•UCLA Round 0 VHDL in verification stage - expected delivery : April 99

•USC/ISI SLAAC II board designed and fabricated, in verification stage - expected completion : April 99

•UCLA Round 0 VHDL will be tested on SLAAC II at ISI : April 99

•NVL Demo with SLAAC II (R0) and CSPI 2641(R1-R5) : May 99